PATENT
8074-1143

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Koichi NANIWE Conf. 9283

Application No. 10/573,492 Group 2892

Filed May 15, 2006 Examiner Eric W. Jones

METHOD OF CLEANING TREATMENT AND METHOD FOR MANFACTURING SEMICONDUCTOR DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents July 8, 2009
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with Rules 1.97 and 1.98, and in fulfillment of the duty of disclosure under Rule 1.56, the accompanying documents, copies of which are attached to this statement, are made of record on the enclosed Form PTO-1449.

A concise explanation of the relevance of these items is that these references were cited by the Japanese Patent Office in the corresponding Japanese Application Serial No. 2002-084968, filed June 20, 2006 and in the corresponding Japanese Application Serial No. 2002-084968, filed July 3, 2007. A copy of the Japanese Official Action in which they were cited is attached hereto, with what is believed to be the pertinent portion enclosed in a wavy line. An English translation of the enclosed portion is also attached hereto.

If necessary, the Commissioner is hereby authorized in

this, concurrent, and future submissions, to charge any underpayment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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